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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,513	10/26/2001	Klaus-Peter Behrens	20 01 0631	6890

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EXAMINER

TORRES, JUAN A

ART UNIT	PAPER NUMBER
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2631

DATE MAILED: 04/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/032,513		BEHRENS ET AL.	
	Examiner		Art Unit	
	Juan A. Torres		2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 October 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>10/06/2001</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto (US 4893072) and further in view of Alston (US 6055285).

As per clam 1 Matsumoto discloses a testing unit for testing a device under test (DUT) comprising a signal generator adapted for applying a stimulus signal to the DUT (figure 5 algorithmic pattern generator ALGP, column 7 lines 45-52) and a receiving unit adapted for receiving a response signal from the DUT on the applied stimulus signal (figure 5 block C Comparator circuit). Matsumoto doesn't disclose a synchronizing unit for synchronizing a data flow of the response signal between the DUT and the receiving unit, the synchronizing unit receives a first clock signal from the DUT and a second clock signal of the testing unit, the synchronizing unit comprising a buffer for buffering data; a write unit for writing data from the DUT into the buffer, where a write access onto the buffer is controlled by the first clock signal; a read unit for reading out data from the buffer to be provided to the receiving unit, a read access onto the buffer is controlled by

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the second clock signal. Alston discloses a synchronizing unit for synchronizing a data flow of the response signal between the DUT and the receiving unit, the synchronizing unit receives a first clock signal from the DUT and a second clock signal of the testing unit, the synchronizing unit (figure 2 column 8 line 57 to column 9 line 12) including a buffer for buffering data (figure 2 blocks 110, 210 and 212 column 6 line 42 and column 8 line 67 to column 9 line 12); a write unit for writing data from the DUT into the buffer, a write access onto the buffer is controlled by the first clock signal (figure 2 blocks 140 column 8 lines 57-62); and a read unit for reading out data from the buffer to be provided to the receiving unit, a read access onto the buffer is controlled by the second clock signal (figure 2 blocks 142 column 8 line 60 to column 9 line 3). Matsumoto and Alston are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Matsumoto with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been to synchronize two clock domains of the signal generator and the response from the DUT (Alston abstract). Therefore, it would have been obvious to combine Matsumoto with Alston to obtain the invention as specified in claim 1.

As per claim 2 Matsumoto and Alston disclose claim 1. Alston also discloses that the buffer comprises a register structure with a plurality of registers (figure 3 blocks 300, 304 and 306 column 9 line 49-50). Matsumoto and Alston are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for

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testing disclosed by Matsumoto with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been to synchronize two clock domains of the signal generator and the response from the DUT (Alston abstract). Therefore, it would have been obvious to combine Matsumoto with Alston to obtain the invention as specified in claim 2.

As per claim 3 Matsumoto and Alston disclose claim 2. Alston also discloses a write pointer adapted to be moved between the pluralities of registers for defining one of the plurality of registers to receive and buffer data from the DUT (figure 2 block 214 column 8 lines 62-66), and a read pointer adapted to be moved between the plurality of registers for defining one of the pluralities of registers to be read out (figure 2 block 216 column 9 lines 4-12). Matsumoto and Alston are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Matsumoto with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been to synchronize two clock domains of the signal generator and the response from the DUT (Alston abstract). Therefore, it would have been obvious to combine Matsumoto with Alston to obtain the invention as specified in claim 3.

As per claim 4 Matsumoto and Alston disclose claim 3. Alston also discloses that the write pointer is adapted to be clocked by the first clock signal for successively writing successive data words from the DUT to different registers (figure 3 block 122 and 106 column 9 lines 34-38), and the read pointer is adapted to be clocked by the

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second clock signal for successively reading out successive data words buffered in the plurality of registers (figure 5 block 132 and 108 column 17 lines 18-21). Matsumoto and Alston are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Matsumoto with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been to synchronize two clock domains of the signal generator and the response from the DUT (Alston abstract). Therefore, it would have been obvious to combine Matsumoto with Alston to obtain the invention as specified in claim 4.

As per claim 5 Matsumoto and Alston disclose claim 1. Alston also discloses that the write unit comprises a latch controlled by the first clock signal, so that successive data words can be latched with the first clock signal and thus successively written into the buffer (figure 3 block 300 column 9 lines 34-40). Matsumoto and Alston are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Matsumoto with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been to synchronize two clock domains of the signal generator and the response from the DUT (Alston abstract). Therefore, it would have been obvious to combine Matsumoto with Alston to obtain the invention as specified in claim 5.

As per claim 6 Matsumoto and Alston disclose claim 1. Alston also discloses that the buffer is adapted to provide an initial delay time between a first valid write access

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and a first valid read access (figure 6 block 310 flip-flops 330-332-334-336 column 17 lines 23-28). Matsumoto and Alston are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Matsumoto with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been to synchronize two clock domains of the signal generator and the response from the DUT (Alston abstract). Therefore, it would have been obvious to combine Matsumoto with Alston to obtain the invention as specified in claim 6.

As per claim 7 Matsumoto and Alston disclose claim 6. Alston also discloses that the initial delay time is provided dependent on the maximum expected variation between such write and read accesses (figure 3 block 310 flip-flops 330-332-334-336 column 7 lines 23-28). Matsumoto and Alston are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Matsumoto with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been to synchronize two clock domains of the signal generator and the response from the DUT (Alston abstract). Therefore, it would have been obvious to combine Matsumoto with Alston to obtain the invention as specified in claim 7.

As per claim 8 Matsumoto discloses a testing method for testing a device under test (DUT), the method comprising the steps of applying a stimulus signal to the DUT

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(figure 5 algorithmic pattern generator ALGP, column 7 lines 45-52); and receiving the read out data in response to the stimulus signal by a receiving unit (figure 5 block C Comparator Circuit, column 7 lines 54-60). Matsumoto doesn't disclose writing data in response to the stimulus signal from the DUT into a buffer, where a write access onto the buffer is controlled by a first clock signal of the DUT, and reading out data from the buffer to be provided to a receiving unit, where a read access onto the buffer is controlled by a second clock signal of the receiving unit. Alston discloses writing data in response to the stimulus signal from the DUT into a buffer, where a write access onto the buffer is controlled by a first clock signal of the DUT (figure 2 blocks 140 column 8 lines 57-62), and reading out data from the buffer to be provided to a receiving unit, where a read access onto the buffer is controlled by a second clock signal of the receiving unit (figure 2 blocks 142 column 8 line 60 to column 9 line 3). Matsumoto and Alston are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Matsumoto with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been to synchronize two clock domains of the signal generator and the response from the DUT (Alston abstract). Therefore, it would have been obvious to combine Matsumoto with Alston to obtain the invention as specified in claim 8.

As per claim 9 Matsumoto and Alston disclose claim 8. Alston also discloses a step of initializing a first valid write access and/or a first valid read access (figure 6 block 310 flip-flops 330-332-334-336 column 17 lines 23-28). Matsumoto and Alston are

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analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Matsumoto with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been to synchronize two clock domains of the signal generator and the response from the DUT (Alston abstract). Therefore, it would have been obvious to combine Matsumoto with Alston to obtain the invention as specified in claim 9.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAT
2-25-2005